

CLAIMS

1. Method for analogue self calibrating of a phase locked loop (PLL) circuit comprising a phase frequency detector (PFD), a charge pump (CP), a loop filter (LPF), a voltage controlled oscillator (VCO), including a plurality of VCO tuned elements, which output signal is compared with a reference signal frequency (F_{ref}) entering in the phase frequency detector (PFD) characterized in that, the voltage controlled oscillator (VCO) operating mode, using a linearized frequency versus voltage curve, is switched, in a first frequency tuning operation enabling a wide locking range, to a linear high gain (LHG) mode, after locking to the appropriate frequency with the said first tuning operation, said voltage controlled oscillator (VCO) operating mode is automatically switched to a zero-gain (ZG) mode while keeping the frequency of said voltage controlled oscillator (VCO) unchanged.
2. Method according to claim 1 characterized in that, after said zero-gain (ZG) mode, said voltage controlled oscillator (VCO) operating mode is switched to a low gain (LG) mode enabling a fine tuning of the frequency by the phase locked loop (PLL) for compensating small residual frequency errors and temperature variations.
3. Method according to claim 1 characterized in that, the voltage controlled oscillator (VCO) frequency versus voltage operating curve linearization comprises following steps:
 - breaking the required linear frequency versus voltage curve FV into several sections fV over either constant or non constant voltage intervals;
 - selecting for each section fV a corresponding VCO tuned element giving the same frequency variation over said section fV ;
 - submitting each VCO tuned element to a specific voltage, deduced from the loop filter (LPF) output tuning voltage, in such way that said VCO tuned element is activated in the same voltage interval as its corresponding section fV .
4. Method according to claim 1 characterized in that the linearization of the voltage controlled oscillator (VCO) frequency versus voltage operating curve is performed during the linear-high gain (LHG) mode.

5. Method according to claim 1 characterized in that switching of the voltage controlled oscillator (VCO) from the linear-high-gain (LHG) mode to the zero-gain (ZG) mode comprises following steps:

- isolating the VCO tuned elements from their controlling voltages when the phase locked loop PLL is locked;
- comparing each VCO tuned element voltage to a reference voltage to determine if the value of said VCO tuned element was at its maximum or its minimum when the phase locked loop PLL was locked;
- depending on the result of this comparison, applying a voltage equal to a specified minimum value or to a specified maximum value to each VCO tuned element, switching its value to its maximum or to its minimum, the total value of said VCO tuned elements is thus equal to their value when the phase locked loop PLL was locked;
- freezing the VCO tuned elements in the state previously obtained to activate thus the zero-gain (ZG) mode for the voltage controlled oscillator (VCO).

6. Method according to claim 2 characterized in that switching of the voltage controlled oscillator (VCO) from the zero-gain (ZG) mode to the low-gain (LG) mode comprises following steps:

- using an additional VCO tuned element that is dimensioned to achieve the needed fine tuning with a low voltage controlled oscillator (VCO) gain;
- linking said VCO tuned element to a fixed voltage during linear-high-gain (LHG) mode and zero-gain (ZG) mode;
- isolating said additional VCO tuned element from this fixed voltage during the switching step from zero-gain (ZG) mode to low-gain (LG) mode;
- linking said additional VCO tuned element to the tuning voltage supplied by the loop filter (LPF) of the phase locked loop PLL;
- achieving the fine tuning operation by the phase locked loop PLL.

7. Method according to claim 2 characterized in that the loop filter (LPF) output voltage is compared to an upper and a lower limit by means of additional comparators during low gain (LG) mode; the tuning operations are restarted and the initial linear high gain (LHG) mode is selected again when the loop filter (LPF) output voltage reaches either of the upper limit or the lower limit.

8. Method according to claim 1 characterized in that the phase locked loop PLL locking time during the linear high gain (LHG) mode is improved by switching off a fraction of the capacitance of the loop filter (LPF) or optionally by increasing the current of the charge pump (CP).

9. Method according to claim 2 characterized in that the phase locked loop PLL stability during the operations at the linear high gain (LHG) and the low gain (LG) modes is preserved by decreasing the charge pump (CP) current during the linear high gain mode (LHG) mode and by increasing said current during the low gain (LG) mode in such way that the product of the charge pump (CP) current and the gain of the voltage controlled oscillator (VCO) remains constant.

10 Integrated circuit comprising a phase locked loop (PLL) circuit including, a phase or frequency detector (PFD) that compares the phase and frequency (F_{ref}) of a reference signal to the phase and frequency of an internal feedback signal and generates output error signals, a charge pump (CP) that generates amounts of charges proportional to said output error signals, a loop filter (LPF) for setting an analogue voltage proportional to the charges accumulated in their capacitors, a voltage-controlled oscillator (VCO) with multiples inputs corresponding each to a VCO tuned element

characterized in that said phase locked loop (PLL) circuit includes a gain mode switcher (GMS) circuit connected between the loop filter (LPF) output and the voltage-controlled oscillator (VCO) inputs, enabling the voltage-controlled oscillator (VCO) to work successively in a linear high-gain (LHG) mode and a zero-gain (ZG) mode; the gain mode switcher (GMS) includes offsets generators (OG) circuits, a switch configuration and comparators (SC); the offsets generators (OG) generate the voltages after shifting the loop filter (LPF) output voltage with predefined offsets; the switch configuration apply the voltages of the offset generators (OG) to the inputs of the voltage-controlled oscillator (VCO) during the linear high gain (LHG) mode, isolates the inputs of the voltage-controlled oscillator (VCO) from the offset generators (OG) and apply the output voltages of said offsets generators (OG) to the inputs of the comparators (SC) during the transition to zero gain (ZG) mode, apply the resulting outputs voltages of said comparators (SC) to the inputs of the voltage-controlled oscillator (VCO), and finally freeze the state of each comparator (SC) and

thus the frequency of the voltage-controlled oscillator (VCO) making it independent on the loop filter (LPF) output voltage, which constitute the zero-gain (ZG) mode.

11 Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 10 characterized in that the VCO tuned elements of the voltage controlled oscillator (VCO) include varactors dimensioned in such a way that the voltage controlled oscillator (VCO) has a relatively constant voltage to frequency gain during the linear high gain (LHG) mode step, each varactor being controlled by a corresponding input of the voltage-controlled oscillator (VCO).

12. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 11 characterized in that the voltage-controlled oscillator (VCO) further comprises, an additional varactor that enables to achieve a fine frequency tuning during the low gain (LG) mode and a switch configuration enabling the application of a constant voltage to said varactor during the linear high gain (LHG) mode and the zero gain (ZG) mode, and the application of the loop filter (LPF) output voltage to said varactor during the low gain (LG) mode.

13. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 10 characterized in that the voltage controlled oscillator (VCO) is constituted by a current controlled oscillator (ICO) which include VCO tuned elements comprising voltage to current converters (V-I) including voltage controlled current sources (VCI) dimensioned in such way that the current controlled oscillator (ICO) has a relatively constant voltage to frequency gain during the linear high gain (LHG) mode step, each controlled current sources (VCI) being controlled by a corresponding input of the voltage-controlled oscillator (VCO).

14. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 13 characterized in that each VCO tuned element further comprises, an additional controlled current sources (VCI) that enables to achieve a fine frequency tuning during the low gain (LG) mode and a switch configuration enabling the application of a constant voltage to said controlled current sources (VCI) during the linear high gain (LHG) mode and the zero gain (ZG) mode, and the application of the loop filter (LPF) output voltage to said controlled source (VCI) during the low gain (LG) mode.

15. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 10 characterized in that it further comprises a lock detector (LD) that activates the switch configuration in such way that: the linear high gain (LHG) mode is selected during a sufficiently long time for the loop to lock and the transition to zero gain (ZG) mode is activated after this locking.

16. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 12 characterized in that it further comprises comparators that set an upper and a lower limit for the loop filter (LPF) output voltage during the low gain (LG) mode and restart the initial linear high gain (LHG) mode when said loop filter output voltage reaches either of these two limits.

17. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 10 characterized in that it further comprises a voltage doubler circuit that increase the voltage supply of the charge pump (CP), the loop filter (LPF) and the offsets generators (OG) during the linear high-gain mode (LHG) and hence enhance the tuning range of the PLL.

18. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 17 characterized in that it further comprises a switch configuration enabling the application of the voltage doubler to the charge pump (CP), the loop filter and the offsets generators (OG) during the linear high-gain mode (LHG) and the output operating voltage supply during the low gain (LG) mode.